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EXAMINER	
KRAVETS, LEONID	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/636,179	Applicant(s) GATZEMEIER ET AL.	
	Examiner Leonid Kravets	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/2003*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Drawings

1. The drawings are objected to because "Global" is misspelled in "Globle Bit Line" of Fig. 1A. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-13, 16, 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Acharya (US Patent 6,055,184) further in view of Bruce et al (US Patent 6,529,416)

As per claim 1, the combination of Acharya and Bruce discloses a method for parallel erase block tagging a plurality of memory devices each having a plurality of memory blocks [Acharya discloses a method of tagging sectors that are subject to a parallel erase operation (Acharya, Col 3, lines 24-26), Bruce discloses performing operations on a plurality of flash memory chips operating in parallel with each other (Col 7 lines 63-64)], the method comprising:

transmitting an erase pulse to the plurality of memory blocks that are not erase

block tagged [Note that in Acharya, the tagged blocks are equivalent to the untagged blocks of the claim (Col3, lines 24-26)]:

determining a memory erase block status for the plurality of memory blocks (Acharya, Col 3, lines 23-24); and

transmitting a parallel erase block tagging data burst to the plurality of memory devices [Bruce describes sending erase command sequences directed at flash chips in a sequential manner by DMA controller on a flash bus, rendering flash bus unavailable during the launching of the commands. A burst is defined as transfer of a block of data all at one time without a break. Thus, Bruce discloses transmitting a parallel erase block tagging data burst to the plurality of memory devices (Col 7, lines 50-54)], the data burst comprising erase block tag patterns for at least one of the memory devices [The data burst of Bruce has erase command sequences (Col 7, line 50), Acharya further discloses erasing sectors that are tagged for erasure (Col 3, lines 24-26)].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the sending of erase commands in parallel to flash chips of Bruce into the system of erasing tagged blocks of Acharya since Bruce and Acharya form the same field of endeavor, namely memory operations and this would allow for faster operation of the memory devices.

As per claim 2, the method of Acharya and Bruce discloses the method of claim 1 wherein determining a memory block status comprises reading each memory cell in a memory block [Acharya discloses the testing method where the erased sectors can be tested to ensure that the memory cells have all been properly erased (Col 8, lines 8-9)].

As per claim 3, the combination of Acharya and Bruce discloses the method of claim 1 wherein writing the parallel erase block tagging data burst to the plurality of memory devices comprises writing a portion of the data burst to a first erase block latch in the at least one memory device [Acharya discloses one tag register associated with each sector utilized to tag a sector for erase, each tag register receives a sector select signal (Col 5, lines 5-7 and 10-12)].

As per claim 4, the combination of Acharya and Bruce discloses the method of claim 3 wherein the portion of the data burst is converted to a logical address of the first erase block latch [Acharya discloses using address signals in a sector decoder circuit to generate sector select signals for the tag registers (Col 5, lines 20-22)].

As per claim 5, the combination of Acharya and Bruce discloses the method of claim 3 and further including continuing to transmit erase pulses to the plurality of memory blocks until all of the erase block latches indicate that the plurality of memory blocks of each of the plurality of memory devices are erased [Acharya discloses that

parallel erase operations of smaller and smaller sets of sectors can be repeated until no sector fails an erase test (Col 3, lines 26-28)].

As per claim 6, the combination of Acharya and Bruce discloses a method for parallel erase block tagging a plurality of memory devices each having a plurality of memory blocks [Acharya discloses a method of tagging sectors that are subject to a parallel erase operation (Acharya, Col 3, lines 24-26), Bruce discloses performing operations on a plurality of flash memory chips operating in parallel with each other (Col 7 lines 63-64)] including a plurality of memory cells (Acharya, Col 3, line 19), each memory block having an erase block latch [Acharya discloses one tag register associated with each sector utilized to tag a sector for erase, each tag register receives a sector select signal (Col 5, lines 5-7 and 10-12)], the method comprising:

Transmitting an erase pulse to the plurality of memory blocks that are not erase block tagged [Note that in Acharya, the tagged blocks are equivalent to the untagged blocks of the claim (Col3, lines 24-26)];

reading the plurality of memory cells to determine the memory erase block status for each of the plurality of memory blocks (Acharya, Col 3, lines 23-24); and

transmitting a parallel erase block tagging data burst to the plurality of memory devices [Bruce describes sending erase command sequences directed at flash chips in a sequential manner by DMA controller on a flash bus, rendering flash bus unavailable during the launching of the commands. A burst is defined as transfer of a block of data all at one time without a break. Thus, Bruce discloses

transmitting a parallel erase block tagging data burst to the plurality of memory devices (Col 7, lines 50-54)], the data burst comprising a plurality of erase block tag patterns [The data burst of Bruce has erase command sequences (Col 7, line 50), Acharya further discloses erasing sectors that are tagged for erasure (Col 3, lines 24-26)], each erase block tag pattern indicating which of the erase block latches to set in response to the memory erase block status [Acharya further discloses erasing sectors that have registers tagged for erasure (Col 5, lines 7-8)].

As per claim 7, the combination of Acharya and Bruce discloses the method of claim 6, and further including programming the plurality of memory blocks prior to transmitting the erase pulses [Acharya discloses that programming and erase operation of an EEPROM can consume considerable time, thus showing that the operations are done as a pair (Col 1, lines 66-67)].

As per claim 8, the combination of Acharya and Bruce discloses the method of claim 6 wherein the plurality of memory devices are flash memory devices (Acharya, Col 2, lines 19-20).

As per claim 9, the combination of Acharya and Bruce discloses the method of claim 8, wherein the plurality of flash memory devices are NAND flash memory devices (Col 8, lines 50-53).

As per claim 10, the combination of Acharya and Bruce discloses the method of claim 8, wherein the plurality of flash memory devices are NOR flash memory devices (Col 5, line 67- Col 6, line 1).

As per claim 11, the combination of Acharya and Bruce discloses a method for parallel erase block tagging a plurality of memory devices in a testing apparatus [Acharya discloses erasing memory blocks for testing of memory, thus in a testing apparatus (Col 2, lines 40-42)], each memory device having a plurality of memory blocks organized into sectors and including a plurality of memory cells (Acharya, Col 3, lines 19), each memory block having an erase block latch (Acharya, Col 5, lines 5-8), the method comprising:

Transmitting an erase pulse to the plurality of memory blocks that are not erase block Tagged [Note that in Acharya, the tagged blocks are equivalent to the untagged blocks of the claim (Col3, lines 24-26)];

reading the plurality of memory cells to determine the memory erase block status for each of the plurality of memory blocks (Acharya, Col 3, lines 23-24);

if at least one memory block is still programmed, generating an erase block tag pattern for each memory block still programmed [Acharya discloses that parallel erase operations of smaller and smaller sets of sectors can be repeated until no sector fails an erase test (Col 3, lines 26-28)].;

generating a plurality of data bursts, each data burst comprised of erase block tag

patterns for a predetermined sector address [In order to transmit a data burst, one must be generated, Bruce describes that erase command sequences are transmitted to the flash chips (Col 7, lines 50-54), Acharya discloses that address signals are sent to a sector decoder which then generates sector select signals to select sectors for erase (Col 5, lines 20-25)];

transmitting the plurality of data bursts to the plurality of memory devices, each erase block tag pattern indicating which of the erase block latches to set in response to the memory erase block status [the data burst of Bruce containing erase command sequences, and the address signals of Acharya indicate which sector registers to erase from those tagged in Acharya]; and

setting the erase block latches in response to the erase block tag patterns [tag registers are utilized to tag a sector for erase, and are selected based on the sector select signals (Col 5, lines 7-8 and 24)].

As per claim 12, the combination of Acharya and Bruce discloses the method of claim 11 and further including translating each erase block tag pattern received in a data burst to a logical address for a predetermined memory device [Acharya discloses using address signals in a sector decoder circuit to generate sector select signals for the tag registers (Col 5, lines 20-22)].

As per claim 13, the combination of Acharya and Bruce discloses an apparatus for parallel erase block tagging (Acharya, Col 3, lines 24-26) comprising:

A plurality of memory devices (Bruce, Col 7, line 51), each memory device comprising a plurality of memory blocks (Acharya, Col 3, lines 18-20, each memory block having an erase block tag latch (Acharya, Col 5, lines 5-6);

A plurality of data input/output lines coupled to the plurality of memory devices (Bruce, Col 4, lines 26-29); and

A processor coupled to the plurality of data input/output lines [Processor is coupled to the flash device through a local bus, attached to a DMA controller, attached to the flash bus for controlling testing operations of the plurality of memory devices (Bruce, Col 4, lines 22-23, Fig. 1, Ref 20, 22, 12, 16)], the processor capable of generating data bursts comprising a plurality of erase block tag patterns that are transmitted to each of the plurality of memory devices in parallel [The processor sends requests through the DMA controller, the requests are directed at flash chips in a sequential manner by DMA controller on a flash bus, rendering flash bus unavailable during the launching of the commands. A burst is defined as transfer of a block of data all at one time without a break. Thus, Bruce discloses a processor generating and transmitting parallel erase block tagging data bursts to the plurality of memory devices (Col 4, lines 21-28, Col 7, lines 50-54)].

As per claim 16, Acharya and Bruce disclose the apparatus of claim 13, wherein the plurality of memory devices are capable of decoding a received erase block tag pattern from a data burst into a logical address corresponding to an erase block tag latch [Acharya discloses that in a flash device a sector decoder circuit receives a

collection of address signals and generates sector select signals that are associated with tag registers of each sector].

As per claim 18, Acharya and Bruce disclose the apparatus of claim 14 wherein each of the plurality of memory devices is capable of setting, substantially simultaneously, a first erase block tag latch in response to a received erase block tag pattern [Bruce discloses transmitting in parallel erase command sequences to flash chips (Col 7, lines 50-52, 63-64) Acharya discloses setting tag registers based on the sector select signal generated by the sector decoder signal (Col 5, 4-8 and 20-22)].

As per claim 19, Acharya and Bruce disclose an electronic system for parallel erase block tagging of memory devices [Bruce discloses performing operations on a plurality of flash memory chips operating in parallel with each other (Col 7 lines 63-64)], the system comprising:

A plurality of memory devices, each memory device comprising a plurality of memory blocks [Acharya discloses a method of tagging sectors that are subject to a parallel erase operation (Acharya, Col 3, lines 24-26)], each memory block having an associated erase block tag latch [Acharya discloses one tag register associated with each sector (Col 5, lines 5-6)];

A plurality of data input/output lines coupled to the plurality of memory devices (Bruce, Col 4, lines 26-29); and

A processor coupled to the plurality of data input/output lines for controlling testing

operations of the plurality of memory devices [Processor is coupled to the flash device through a local bus, attached to a DMA controller, attached to the flash bus for controlling testing operations of the plurality of memory devices (Bruce, Col 4, lines 22-23, Fig. 1, Ref 20, 22, 12, 16)], the processor capable of transmitting an erase pulse to the plurality of memory blocks that are not erase block tagged (The processor of Bruce sends requests to the memory through the DMA controller, Acharya teaches erasing the sectors that are tagged for erasure (Col3, lines 24-26), this is equivalent to sending an erase pulse to the memory blocks that are not erase block tagged of the present claim], determining a memory erase block status for the plurality of memory blocks (Acharya, Col 3, lines 23-24), and transmitting a parallel erase block tagging data burst substantially simultaneously to the plurality of memory devices, the data burst comprising erase block tag patterns for setting an associated erase block tag latch in the plurality of the memory devices [The processor sends requests through the DMA controller, the requests are directed at flash chips in a sequential manner by DMA controller on a flash bus, rendering flash bus unavailable during the launching of the commands. A burst is defined as transfer of a block of data all at one time without a break. Thus, Bruce discloses a processor generating and transmitting parallel erase block tagging data bursts to the plurality of memory devices (Col 4, lines 21-28, Col 7, lines 50-54). Acharya discloses decoding the tag patterns (address) to set erase block tag registers for erasure (Col 5, lines 20-24)].

As per claim 20, Bruce and Acharya disclose the system of claim 19 wherein an erase block tag latch is set when it has a logic high state (Col 5, lines 7-9).

As per claim 21, Bruce and Acharya disclose a method for parallel erase block tagging a plurality of memory devices each having a plurality of memory blocks including a plurality of memory cells [Acharya discloses a method of tagging sectors that are subject to a parallel erase operation (Acharya, Col 3, lines 24-26), each sector having memory cells (Col 3, line 19), Bruce discloses performing operations on a plurality of flash memory chips operating in parallel with each other (Col 7 lines 63-64)], each memory block having an erase block latch (Col 5, lines 5-6), the method comprising:

Transmitting an erase pulse to the plurality of memory blocks that are not erase block tagged [Note that in Acharya, the tagged blocks are equivalent to the untagged blocks of the claim (Col3, lines 24-26)];

Reading the plurality of memory cells to determine the memory erase block status for each of the plurality of memory blocks (Acharya, Col 3, lines 23-24); and

Transmitting a parallel erase block tagging data burst to the plurality of memory devices [Bruce describes sending erase command sequences directed at flash chips in a sequential manner by DMA controller on a flash bus, rendering flash bus unavailable during the launching of the commands. A burst is defined as transfer of a block of data all at one time without a break. Thus, Bruce discloses

transmitting a parallel erase block tagging data burst to the plurality of memory devices (Col 7, lines 50-54)], the data burst comprising a plurality of erase block tag patterns [The data burst of Bruce has erase command sequences (Col 7, line 50), Acharya further discloses erasing sectors that are tagged for erasure (Col 3, lines 24-26)] each having an equivalent logical state such that when the plurality of memory devices receive the erase block tag patterns, the erase block latches are set to a predetermined state (Acharya, Col 5, lines 7-10).

As per claim 22, the combination of Acharya and Bruce discloses the method of claim 21 wherein the predetermined state is an erased state [In the system of Acharya, the tagged registers indicate the sector is to be erased, but the scope of the specification is not limited to this and it is therefore obvious that the opposite state would also work in the same manner (Acharya, Col 5, lines 7-10)].

As per claim 23, the combination of Acharya and Bruce discloses the method of claim 21 wherein the predetermined state is an unerased state [In the system of Acharya, the tagged registers indicate the sector is to be erased and is thus in an unerased state (Acharya, Col 5, lines 7-10)].

As per claim 24, the combination of Acharya and Bruce discloses the method of claim 21 wherein the equivalent logical state is a logic low [In the system of Acharya,

when all the registers are a logic low, they are de-selected and thus will not be erased (Acharya, Col 5, lines 7-10)].

5. Claims 14, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Acharya in view of Bruce as applied to claim 13 above, and further in view of Mihara (US Patent 6,735,119).

As per claim 14, the combination of Acharya and Bruce teaches the apparatus of claim 13. Acharya and Bruce do not teach including a plurality of bit line drivers, each bit line driver coupled between a data input/output line and a memory device. Mihara discloses such a bit line driver [Mihara discloses that in a conventional EEPROM data is latched from input/output port to all data latch circuits and the potential is raised by a bit line driver before being written into a memory cell (Col 1, lines 42-48)].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the bit line drivers of Mihara into the system of Acharya and Bruce since Acharya, Bruce and Mihara form the same field of endeavor, namely nonvolatile semiconductor devices, further by applicant's admission, bit line drivers are well known in the art.

As per claim 15, the combined system of Acharya, Bruce and Mihara discloses the apparatus of claim 14 and further including a plurality of data latches, each data

latch coupled between a data input/output and a bit line driver [Mihara discloses that in a conventional EEPROM data is latched from input/output port to all data latch circuits and the potential is raised by a bit line driver before being written into a memory cell (Col 1, lines 42-48)].

As per claim 17, the combined system of Acharya and Bruce discloses the apparatus of claim 13. They do not disclose a plurality of bit line drivers coupled to global bit lines of the memory device. Global bit lines and bit line drivers are well known in the art and their use is established. Further, Bruce discloses a bit line driver in his flash bus (Fig.1, Ref 18). Mihara discloses use of bit line drivers to raise the potential of bits (Col 1, lines 46-48). Acharya further discloses that the plurality of erase block tag patterns are transmitted to the plurality of erase block latches [collection of address signals are sent to the sector decoder circuit which generates sector select signals for the tag registers (Col 5, 20-25)].

Conclusion

6. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Harari (US Patent 5,999,446) discloses a flash EEPROM system with multi-sector erase in parallel.

Naso (US PG Pub. 2002/0063500) discloses a flash memory sector tagging method

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on M-F, 8-4:30.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonid Kravets
Patent Examiner
Art Unit 2189

August 30, 2005